A Site Observation Directed Test Pattern Generation Method for Reducing Defective Part Level

Michael R. Grimaila, Sooryong Lee, Jennifer Dworak, M. Ray Mercer, and Jaehong Park

Department of Electrical Engineering
Computer Engineering Group
Texas A&M University
College Station, Texas 77843-3128
TELEPHONE: (409) 862-3360
FAX: (409) 845-2630
EMAIL: mercer@ee.tamu.edu

A Site Observation Directed Test Pattern Generation Method for Reducing Defective Part Level

Abstract

Traditional testing methods attempt to maximize the number of single stuck-at faults detected by the test pattern set applied to minimize defective part level after IC manufacture and prior to shipment. However, stuck-at faults no longer map closely to actual defects in current CMOS technologies. This work optimizes the probability of defect detection -- in contrast to the stuck-at fault detection.

I. Introduction

The goal of the research was to develop a method to improve the ATPG targeting for enhanced detection of manufacturing defects in integrated circuits. Although stuck-at fault detection is widely accepted in industry as a key test quality figure of merit, it does not account for the necessity of detecting other defect types seen in real manufacturing environments. Other researchers have addressed this problem by using defect models during the ATPG process. In this case, the fault simulation engine is modified to allow the simulation of the defect models used to emulate real defects encountered in the manufacturing process. Unfortunately, using defect models during the ATPG process is too costly in both time and memory [FERG91][MAX92][MEI74][MILL88]. Our preliminary investigation showed that valuable information is discarded during the fault simulation phase of the traditional ATPG process. Specifically, each site's fault detection profile is discarded in modern fault simulators because they use fault dropping for time/space efficiency. However, there is a strong correlation between the number of times a fault site is "observed" and the ability of that test set to screen out defects involving that site. In an attempt to quantify the defect reduction, we constructed a new defective part level model that accounts for each individual site's stuck-at fault detection profile as a measure of how well a test vector set can detect manufacturing defects.

Our research differs from existing work in the way that it attempts to reduce the overall defective part level. In our method, we use a standard stuck-at fault model ATPG, but we modify the fault simulator to keep track of each node's stuck-at fault detection profile. The sum of stuck-at one detects and the stuck-at zero detects for a given site is called the site "observation count." By dynamically targeting test vector generation toward the least observed sites and using random decision ATPG, we effectively reduce the overall defective part level of the device. When a fault is detected multiple times given different justification or propagation conditions, we have a higher probability of detecting most of the various defects involving that fault site. A key benefit of this approach is that no defect models except for stuck-at faults are required to direct the ATPG process.

An experiment was designed and conducted using the ISCAS85 benchmark circuits. Non-feedback bridging faults were selected as the defect model to inject into the design, and their ability to be detected was deemed a measure the effectiveness of the generated test sets [BUTL90]. A popular academic ATPG tool called "ATALANTA" was used to provide test generation capability for a given stuck-at fault [LEE93]. A tool was developed to provide the non-fault dropping stuck-at and the bridging fault simulation required for this research. An analysis of the results of the experiment supports our conjecture that increasing each site's observability reduces the overall defective part level of the device.

II. The Role of Excitation and Observation in Defect Detection

Generating tests using the stuck-at fault model requires deterministic excitation and deterministic observation. In Figure 1, a simple circuit is used to illustrate the steps required to generate a test for A stuck-at 1. In this case, A is set to a 0 to excite the fault and S is set to a 1 to allow the fault, D, to propagate through NAND gate N1. Since the signal S is set to a one, the output of inverter I1 is a 0. This zero insures that the output of gate N2 is a one, which allows the D on the output of N1 to propagate to the output of N3 as a D bar. In this case, it does not matter what value is assigned to node B and the resulting value at the output of I2 because this value is blocked from propagating through N3 due to the 0 on the output of I1. Given the conditions that A is equal to 0 and that S is equal to 1, we find that the probability of both the excitation and the observation of fault A stuck-at 1 is equal to 1.

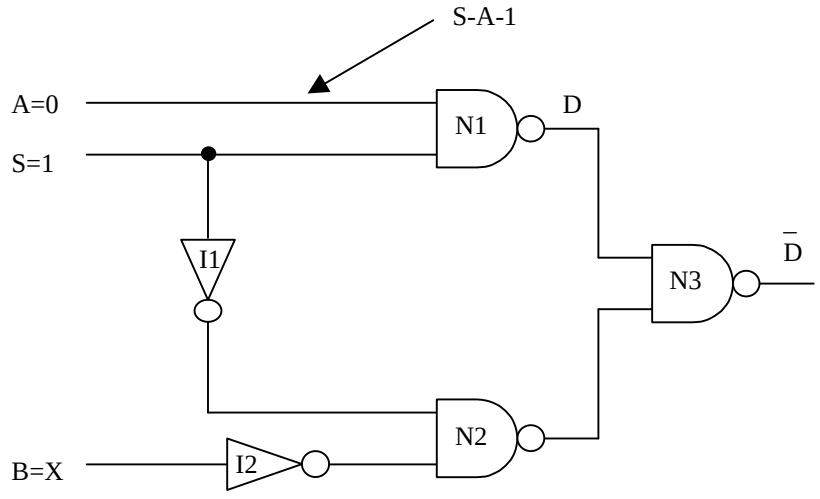


Figure 1 – Example circuit with a test for node A stuck-at 1

If we apply the same test vector to the circuit shown in Figure 2 which contains an OR bridge between node A and node B, we find that the value of node B will determine if the OR bridge is detected or not. If B is equal to 0, the OR bridge is not detected. If B is equal to a 1, then the OR bridge is detected. Given the conditions that A is equal to 0 and

that S is equal to 1, we find that the probability of excitation of the OR bridge fault in this example is ½. Thus, we propose that the excitation for a bridge fault when using a stuck-at fault model for test generation can be probabilistic.

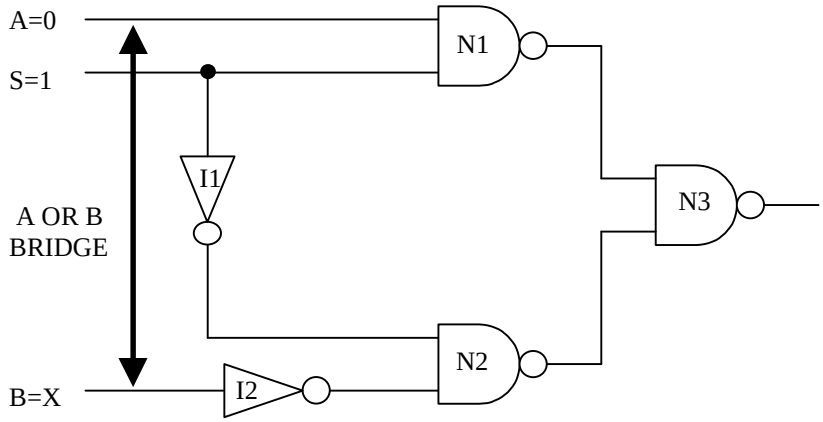


Figure 2 – Example circuit with A OR B bridge fault

If we apply the same test vector to the circuit shown in Figure 3 which contains an OR bridge between node A and node BN, we find that the value of node BN will determine if the OR bridge is detected or not. If BN is equal to 0, the OR bridge is not detected. If BN is equal to a 1, then the OR bridge is detected. Given the conditions that A is equal to 0 and that S is equal to 1, we find that the probability of excitation of the OR bridge fault in this example is ½.

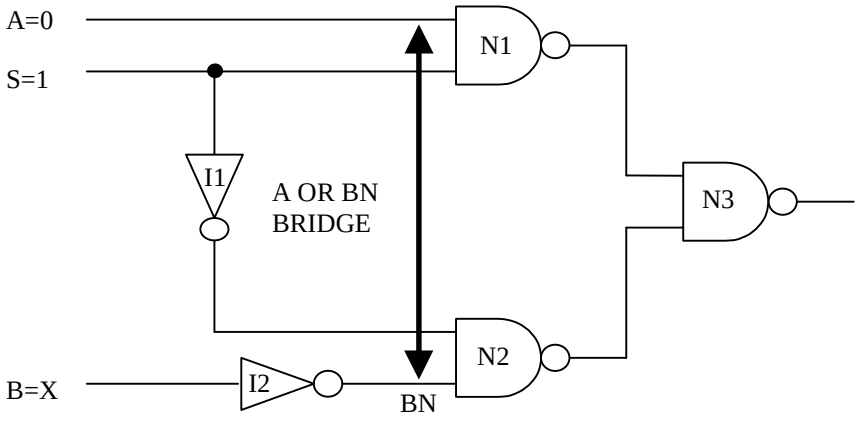
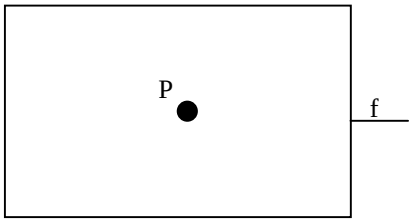


Figure 3 – Example circuit with A OR BN bridge fault

Figure 4 shows a generalized view of test generation criteria for both a P stuck-at one fault and for a generic defect. For the case of a stuck-at fault, both the excitation and propagation conditions are deterministic. In contrast, the test for a node P that has a defect associated with it will have the same deterministic observation, but the probability of defect excitation depends upon the particular character of the defect.



$$T_{P/1} = \overline{P} * \frac{\partial f}{\partial P}$$

$$T_{DEFECT} = \left\{ \begin{matrix} \text{Probabilistic} \\ \text{Excitation} \end{matrix} \right\} * \frac{\partial f}{\partial P}$$

Figure 4 – A comparison between deterministic and probabilistic fault excitation

The conclusion is that stuck-at based testing is deterministic, but other defects can be deterministically observed and probabilistically excited.

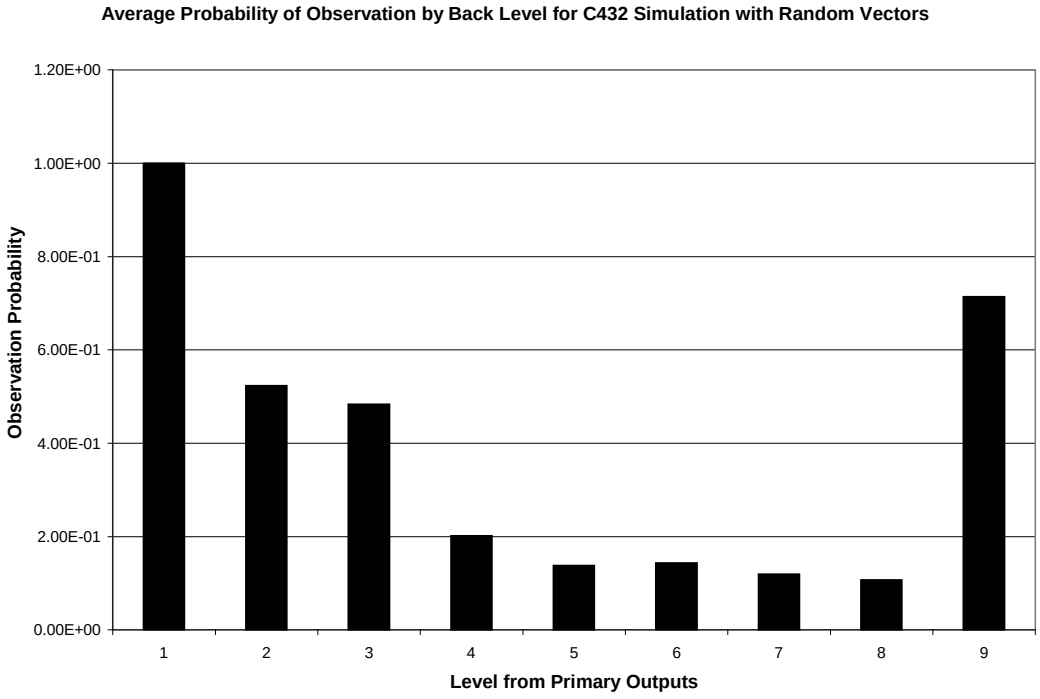


Figure 5 – Average probability of observation as a function of back level in C432 using random vectors

In Figure 5, we see the average probability of observation as a function of the circuit back level in the C432 circuit. The data shows that probability of observation, and hence, the defect detection is greatest near the primary outputs and decreases dramatically as the distance from primary outputs increases.

We now consider the question: "Is the observation or excitation condition dominant?" To gain some insight into answering this question, consider Figure 6 which was created from data collected from the analysis of the circuit C432.

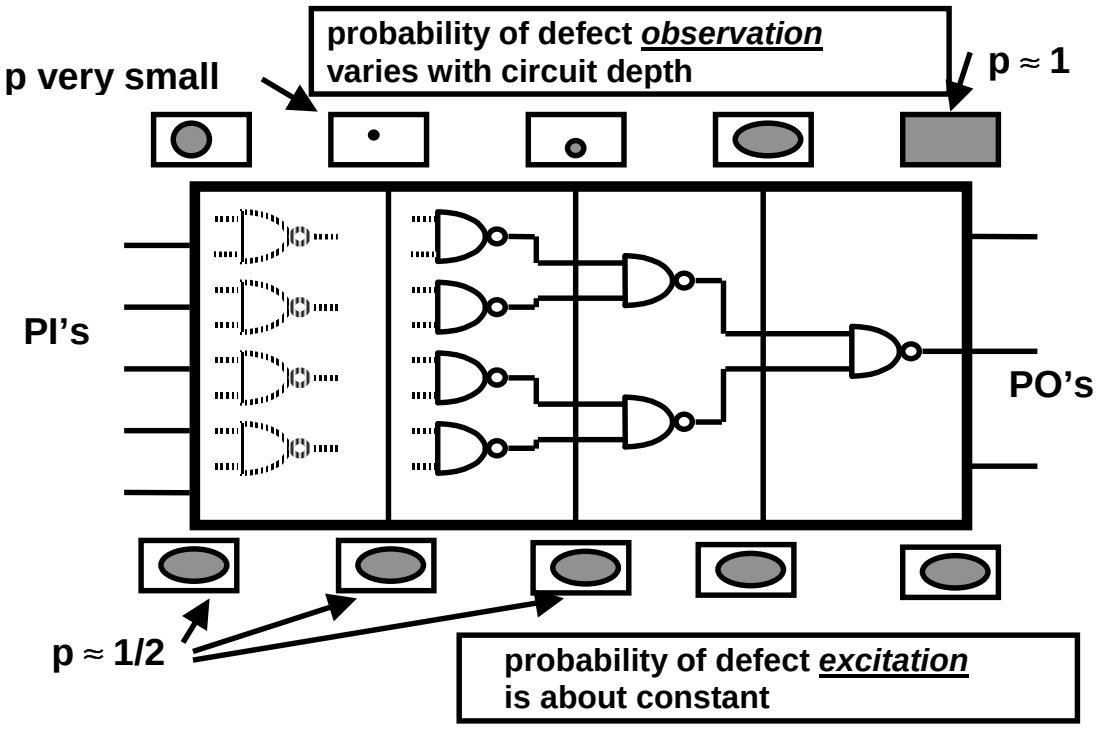


Figure 6 – Probability of excitation and observation as a function of level in C432

Note that the probability of excitation is approximately constant independent of the level of the circuit. In contrast, we find that the probability of observation is large when near the primary outputs of the circuit and drops significantly as that distance increases. Thus, while the probability of excitation is roughly constant across the circuit, the probability of observation varies widely at different circuit locations.

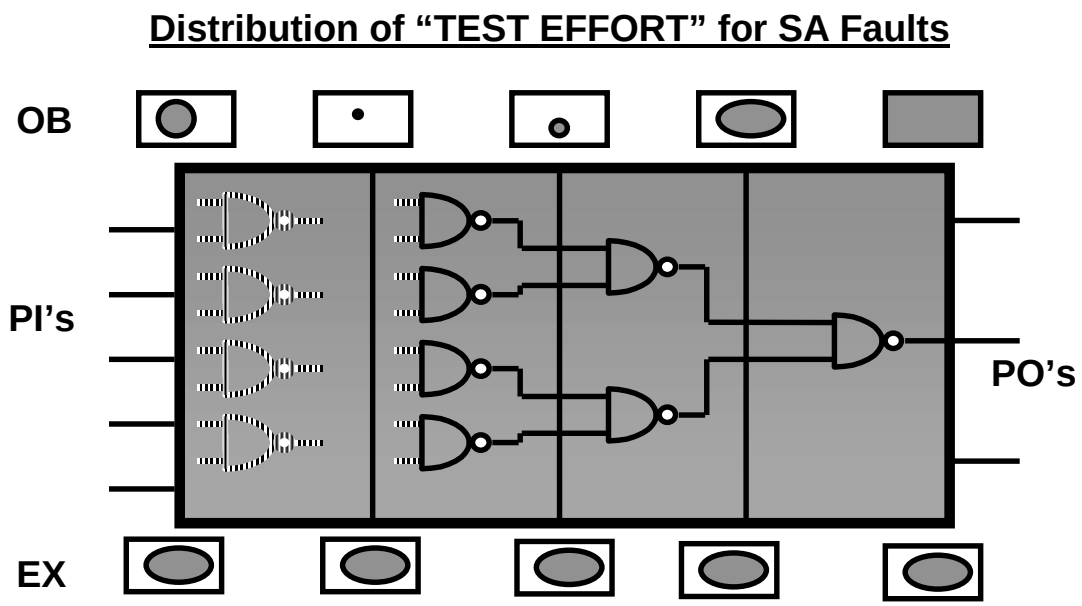


Figure 7 – Test effort as a function of level in C432

The circuit shading in Figure 7 is intended to show that when the standard stuck-at fault model is used during the test generation process, the test effort is equally distributed across the circuit. Thus, sites near primary outputs are regularly observed, and the probability of detection of all defects associated with these sites is very close to one. For sites that are rarely observed, the probability of defect detection is dramatically lower.

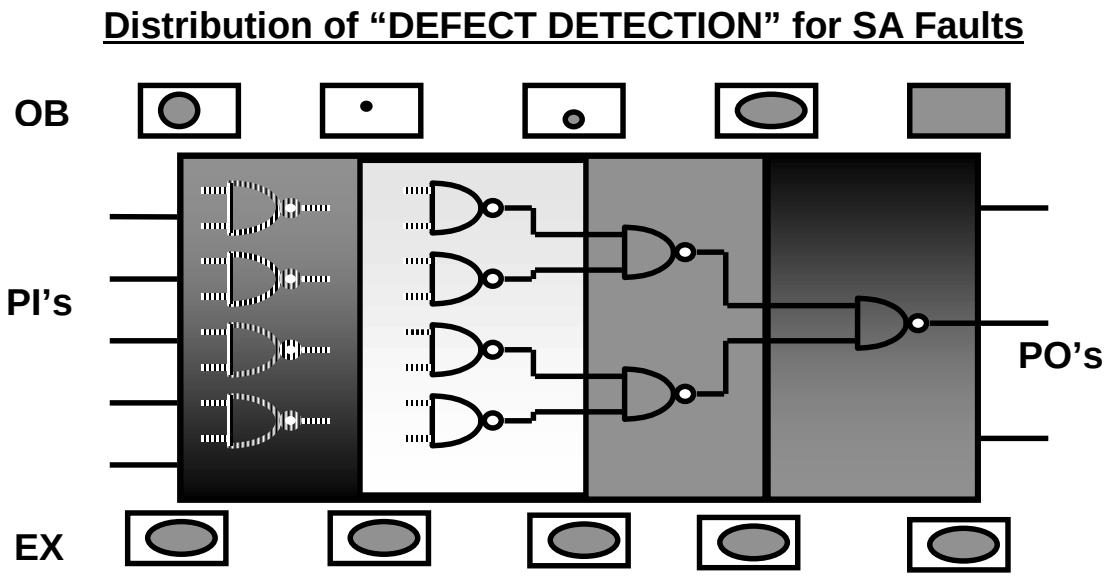


Figure 8 – Defect detection distribution as a function of level in C432

The circuit shading in Figure 8 shows the resulting defect level reduction when uniform effort is applied across the entire circuit. The dark areas are effectively tested for most defects while the lighter areas will be the sites of most undetected defects. By concentrating the testing effort at poorly observed sites, a more effective test pattern set will be produced.

III. A New Defective Part Level Model

In this section, we present a new defective part level model that relates the number of times each fault site is observed and the defective part level. For this work, we assume a constant base probability of excitation, P_{EXCITE}, and a constant probability of the existence of a defect, P_{DEFECT}. We now examine each component of the model.

The number of times a site is observed, $\#OBS_i$, is the sum of stuck at one and stuck at zero fault detections for that site. Notice that the probability of not detecting the fault, $(1-P_{EXCITE})^{\#OBSi}$, is reduced as a site is observed more frequently. The product term $(1-P_{EXCITE})^{\#OBSi}*P_{DEFECT}$ represents the probability of escape, that is, the probability that a defect occurs but is not detected. This model assumes statistical independence between the probability of excitation and the probability of the existence of a defect. If we subtract the probability of escape from one for each site, we obtain the probability that an escape does not occur for that site. The product over all sites of the probability that an escape does not occur is the probability that no escape occurs for the complete circuit. The defective part level is then determined as the ensemble probability that at least one escape occurs. The new defective part level model is shown in Figure 9:

$$DL \cong 1 - \prod_{i=1}^{Sites} \left[1 - \left(1 - P_{EXCITE}\right)^{\#OBS_i} P_{DEFECT} \right]$$

$$P_{EXCITE} \equiv \text{Probability a fault is excited given that the fault is observed (Assumed constant)}$$

$$\left(1 - P_{EXCITE}\right)^{\#OBS_i} \equiv \text{Probability fault } i \text{ is never detected}$$

$$P_{DEFECT} \equiv \text{Probability of a defect at site } i$$

$$P_{DEFECT} \text{ is calculated from: } Yield = \left(1 - P_{DEFECT}\right)^{\#Sites}$$

Figure 9 – A new defective part level model

This model has several advantages when compared with existing stuck-at fault based defect level models. For example, in the traditional models, the defective part level is predicted to be zero when the stuck-at fault coverage reaches 100% [SETH84][WILL81]. In contrast, this new model approaches but never actually reaches a defective part level of zero. The new model uses observation information which is calculated as part of stuck-at fault simulation, and its predictions vary based upon the number of observations which occur at any given site. The actual probability of excitation of an as yet undetected defect during the testing process will monotonically decrease, so that the constant probability of

excitation assumption results in a conservative upper bound for the actual defective part level achieved. Alternatively, the probability of excitation can be modeled as a function of the number of observations at each individual site.

IV. A New Test Generation Method for Defect Level Minimization

Based upon the defective part model given above, a family of new test generation methods have been developed and evaluated. In each case, tests are produced by traditional ATPG algorithms targeting traditional stuck-at faults. The only non-standard requirement on the ATPG algorithm is that the test pattern generation decision process be random so that if the same fault is used twice as a target, the resulting two tests will be non-duplicated, random samples from the set of all possible test patterns for the fault.

In contrast to traditional fault selection methods (such as testing for each undetected fault at least once), we select faults to be targeted in such a way as to maximize the number of times that sites are observed. More specifically, since those sites which are least often observed make the dominant contribution to the defective part level, our objective is to maximize the number of observations of "hard to observe" sites. This means that many stuck at faults will never be used as targets -- because they are often detected by tests targeted at other faults. In contrast, some stuck-at faults will be targeted many times because they are located at sites which are only rarely observed.

Figure 10 shows a generic flow chart for the test pattern generation methods studied. The key differences from standard approaches are: (1) that the least detected fault is always selected for processing next, and (2) fault detection statistics are saved which record how many time each fault has been detected to date.

Initially, all faults have been detected exactly zero times. From this set, one is randomly selected and used as a target to produce the first test pattern. After fault simulation, many faults may have one detection; of the faults with zero detections, another is randomly selected as the next target. Eventually, every fault has been detected at least once, but the process continues by finding the set of faults which have been least detected and randomly selecting one of them as the next target. In some cases, no test is produced because an upper bound on ATPG time is exceeded, and the corresponding fault is removed as a candidate target to avoid excessive ATPG times.

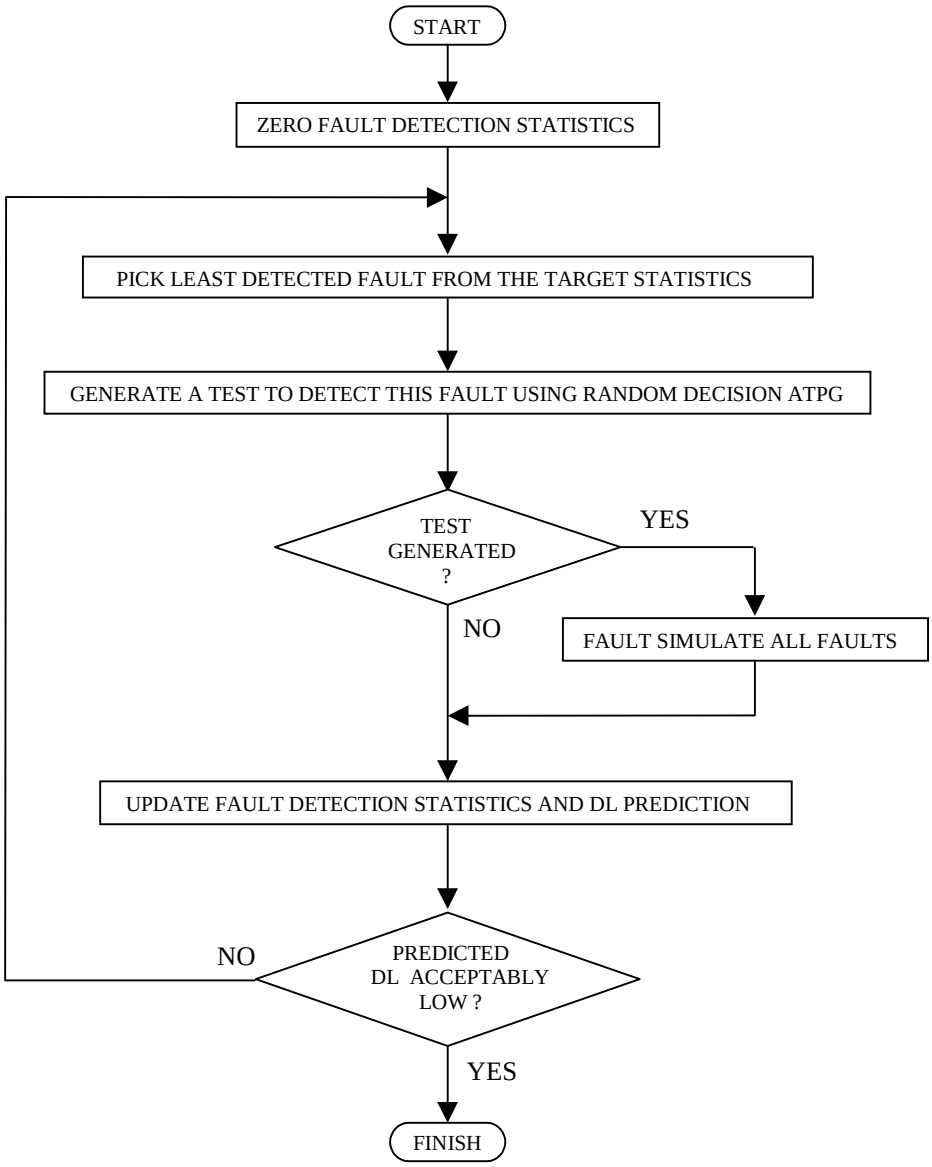


Figure 10 – Dynamic least detected fault targeting algorithm

As usual, there are many variations on the basic theme, and in the result section which follows, three such variations are described, and their performance is compared in a defect simulation experiment.

V. Experimental Design and Results

In order to evaluate the effectiveness of test pattern sets produced based upon the new defective part level model, a simple set of experiments were conducted using the ISCAS benchmark circuit -- C432. All stuck-at one and stuck-at zero faults, after equivalent fault collapse, were used as the basic fault set, and statistics on the number of detections of each fault were monitored during the test pattern generation and fault simulation process. The yield was assumed to be 90%. A total of 45,000 AND and OR bridges between lines in the C432 circuit were modeled, and the defective part level which was determined based upon the number of bridges which remained undetected is shown on the Y axis. Three methods were used to produce test pattern sets, and the results obtained are shown for comparison in Figure 10.

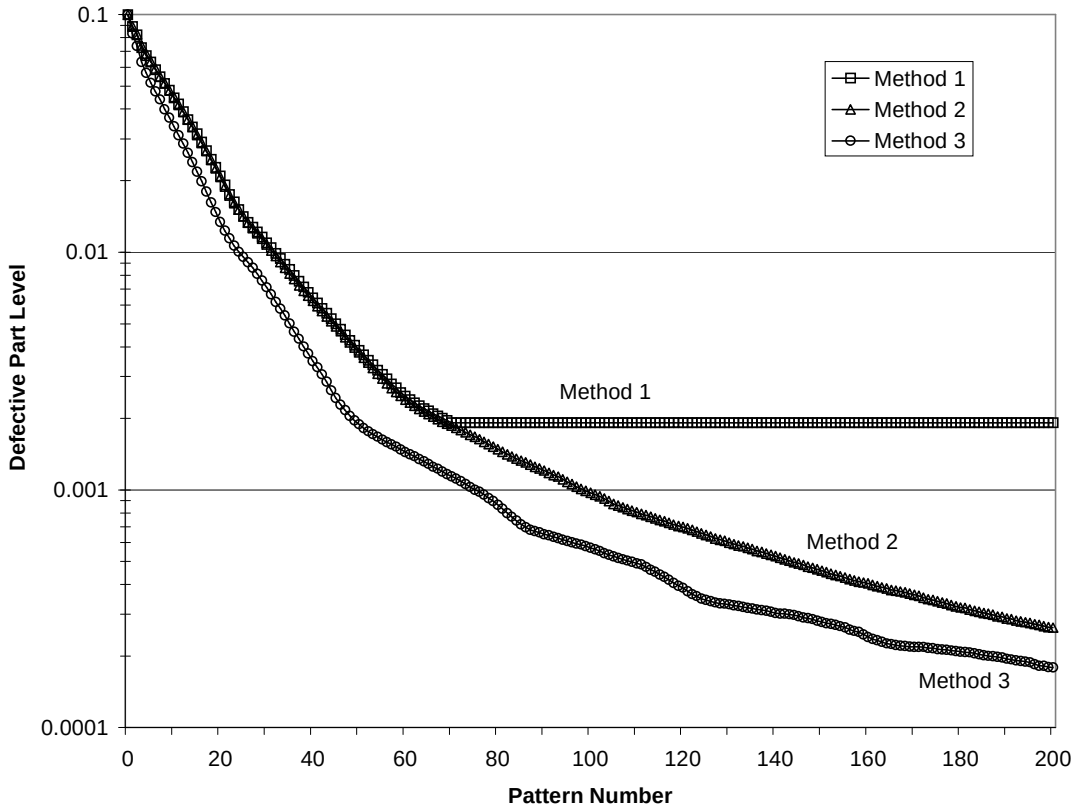


Figure 10 – Defective part level versus pattern number for three different ATPG methods

Method 1 corresponds to traditional industrial practice today. A test pattern set is produced by targeting one currently undetected fault, doing fault simulation, and dropping all detected faults from future consideration as targets. This process is repeated until every detectable fault has been either explicitly targeted and detected or fortuitously detected by a test for some other target fault. At the end of 70 test patterns, the fault coverage is 100% and the process terminates. The resulting defective part level is about 2,000 parts per million.

Method 2 corresponds to the dynamic least detected fault targeting described in the flow chart of Figure 9. In this case, the test generation process was terminated after 200 test patterns were generated, and the resulting defective part level is about 300 parts per million.

Method 3 is similar to method 2 except that after a test pattern has been produced by the ATPG algorithm, it may contain one or many unspecified primary input values (assigned as "X" values). We produce up to 32768 different patterns by random assignments of 0 and 1 to the X's and fault simulate all of them. The test pattern which maximizes the number of fault detections is selected at the test pattern to be included in the final test pattern set. In all, 200 test patterns were generated. This approach was used to understand the level of improvement which could be expected if the test pattern generation effort was increased by several orders of magnitude. It attempts to find an upper bound on the best possible test pattern set targeted exclusively based upon fault detection statistics. The resulting defective part level is about 200 parts per million.

VI. Conclusions

We have presented a new testing method for the reduction of defective part levels in digital integrated circuits. This improvement simply involves using traditional ATPG and fault simulation tools in a new way. By maximizing the deterministic observation of defect sites in the network (as determined from traditional stuck-at fault simulation) and relying upon probabilistic defect excitation, significant improvements in test pattern efficiency have been achieved. In particular, an increase by a factor of three in test pattern set length and superior target fault selection criteria reduced the defective part level by almost one order of magnitude. Perhaps an additional 33% reduction can be achieved by more sophisticated and computationally expensive test pattern selection methods.

VII. References

[BUTL90] Butler, K.B. and Mercer, M.R. "The influences of fault type and topology on fault model performance and the implications to test and testable design," Proc. 27th ACM / IEEE Design Automation Conference 1990.

[FERG91] Ferguson, F.J. and Larrabee, T. "Test pattern generation for realistic bridge faults in CMOS Ics," Proc. International Test Conference 1991, pp. 492-499.

[LEE93] Lee, H.K. and Ha, D.S., "On the generation of test patterns for combinational circuits," Technical Report No. 12, Department of Electrical Engrineering, Virginia Polytechnic Institute and State University, 1993.

[MAX92] Maxwell, P.C. and Aitken, R.C. "I_{DDQ} Testing as a Component of a Test Suite: The Need for Several Fault Coverage Metrics," Journal of Electronic Testing 3, pp. 305-316.

[MEI74] Mei, K.C. "Bridging and stuck-at faults," IEEE Trans. on Computers, Vol. C-23, no. 7, 1974.

[MILL88] Millman, S.D. and McCluskey, E.J. "Detecting bridging faults with stuck-at test sets," Proc. International Test Conference 1988.

[SETH84] Seth, S.C. and Agrawal, V.D. "Characterizing the LSI Yield from Wafer Test Data," IEEE Trans. on CAD, Vol. CAD-3, 1984, pp. 123-126.

[WILL81] William, T.W. and Brown, N.C. "Defect level as a function of fault coverage," IEEE Trans. on Computers, Vol. C-30, no. 12, 1981.